Refine Search

Search Results -

Terms	Documents
L2 and switch	425

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L3

Refine Search

Recall Text | Clear | Interrupt

Search History

DATE: Monday, July 18, 2005 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L3	L2 and switch	425	L3
L2	L1 same memory same cache	808	L2
L1	((disk or disc) near5 controller) same interface	9740	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
L3	0

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L4

Refine Search

Recall Text | Clear | Interrupt

Search History

DATE: Monday, July 18, 2005 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L4	L3	0	L4
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L3	L2 and switch	425	L3
L2	L1 same memory same cache	808	L2
L1	((disk or disc) near5 controller) same interface	9740	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
(709/229 |709/232 |709/253 |710/313 |710/316 |710/104 |710/74 |710/1 |710/305 |711/112 |711/113 |711/114 |711/147 |711/148 |711/130 |714/3 |714/7).ccls.	13526

Database:
- US Pre-Grant Publication Full-Text Database
- US Patents Full-Text Database
- US OCR Full-Text Database
- EPO Abstracts Database
- JPO Abstracts Database
- Derwent World Patents Index
- IBM Technical Disclosure Bulletins

Search: L5

Refine Search

Recall Text | Clear | Interrupt

Search History

DATE: Monday, July 18, 2005 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L5	710/313,316,104,74,1,305;711/112-114,147,148,130;714/3,7;709/229,232,253.ccls.	13526	L5
DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L4	L3	0	L4
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L3	L2 and switch	425	L3
L2	L1 same memory same cache	808	L2
L1	((disk or disc) near5 controller) same interface	9740	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
L6 and (request near5 computer)	77

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L8

Refine Search

Recall Text | Clear | Interrupt

Search History

DATE: Monday, July 18, 2005 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L8	L6 and (request near5 computer)	77	L8
L7	L6 and computer	170	L7
L6	l3 and L5	172	L6
L5	710/313,316,104,74,1,305;711/112-114,147,148,130;714/3,7;709/229,232,253.ccls.	13526	L5
DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L4	L3	0	L4
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L3	L2 and switch	425	L3
L2	L1 same memory same cache	808	L2
L1	((disk or disc) near5 controller) same interface	9740	L1

END OF SEARCH HISTORY

Results for "(disk or disc<in>metadata) <and> (memory<in>metadata) <and> (cache<i..."

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Your search matched **96** of **1193303** documents.

A maximum of **100** results are displayed, **25** to a page, sorted by **Relevance** in **Descending** order.

» View Session History

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Modify Search

(disk or disc<in>metadata) <and> (memory<in>metadata) <and> (cache<in>meta

Check to search only within this results set

Display Format: Citation Citation & Abstract

» Key

IEEE JNL	IEEE Journal or Magazine
IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

Select Article Information

View: **1-25** | 26-50 | 51-75 | 76-96

1. **The design and verification of the Rio file cache**
Ng, W.T.; Chen, P.M.;
Computers, IEEE Transactions on
Volume 50, Issue 4, April 2001 Page(s):322 - 337
AbstractPlus | References | Full Text: PDF(388 KB) IEEE JNL

2. **Multiprocessor memory reference generation using Cerberus**
Rothman, J.B.; Smith, A.J.;
Modeling, Analysis and Simulation of Computer and Telecommunication Systems, 1999. Proceedings. 7th International Symposium on
24-28 Oct. 1999 Page(s):278 - 287
AbstractPlus | Full Text: PDF(172 KB) IEEE CNF

3. **Feedback-based dynamic voltage and frequency scaling for memory-bound real-time applications**
Poellabauer, C.; Singleton, L.; Schwan, K.;
Real Time and Embedded Technology and Applications Symposium, 2005. RTAS 2005. 11th IEEE
7-10 March 2005 Page(s):234 - 243
AbstractPlus | Full Text: PDF(480 KB) IEEE CNF

4. **MUTABOR, a coprocessor supporting memory management in an object-oriented architecture**
Kaiser, J.;
Micro, IEEE
Volume 8, Issue 5, Oct. 1988 Page(s):30 - 46
AbstractPlus | Full Text: PDF(1252 KB) IEEE JNL

5. **The Aquarius-IIU system**
Busing, D.R.; Srini, V.P.; Smine, G.E.; Carlton, M.J.; Despain, A.M.;
Systems Integration, 1990. Systems Integration '90., Proceedings of the First International Conference on
23-26 April 1990 Page(s):38 - 46
AbstractPlus | Full Text: PDF(756 KB) IEEE CNF

6. **An analysis of database workload performance on simultaneous multithreaded processors**
Lo, J.L.; Barroso, L.A.; Eggers, S.J.; Gharachorloo, K.; Levy, H.M.; Parekh, S.S.;
Computer Architecture, 1998. Proceedings. The 25th Annual International Symposium on
27 June-1 July 1998 Page(s):39 - 50
AbstractPlus | Full Text: PDF(196 KB) IEEE CNF

7. **A new memory monitoring scheme for memory-aware scheduling and partitioning**
Suh, G.E.; Devadas, S.; Rudolph, L.;
High-Performance Computer Architecture, 2002. Proceedings. Eighth International Symposium on

2-6 Feb. 2002 Page(s):117 - 128

AbstractPlus | Full Text: PDF(378 KB) IEEE CNF

8. **Making LRU Friendly to Weak Locality Workloads: A Novel Replacement Algorithm to Improve Buffer Cache Performance**
Song Jiang; Xiaodong Zhang;
Computers, IEEE Transactions on
Volume 54, Issue 8, Aug. 2005 Page(s):939 - 952

AbstractPlus | Full Text: PDF(1096 KB) IEEE JNL

9. **A 512 K-bit magneto resistive memory with switched capacitor self-referencing sensing**
Ranmuthu, I.W.; Ranmuthu, K.T.M.; Kohl, C.; Comstock, C.S.; Hassoun, M.;
Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on [see also Circuits and Systems II: Express Briefs, IEEE Transactions on]
Volume 39, Issue 8, Aug. 1992 Page(s):585 - 587

AbstractPlus | Full Text: PDF(260 KB) IEEE JNL

10. **Sequoia: a fault-tolerant tightly coupled multiprocessor for transaction processing**
Bernstein, P.A.;
Computer
Volume 21, Issue 2, Feb. 1988 Page(s):37 - 45

AbstractPlus | Full Text: PDF(828 KB) IEEE JNL

11. **External sorting: run formation revisited**
Larson, P.A.;
Knowledge and Data Engineering, IEEE Transactions on
Volume 15, Issue 4, July-Aug. 2003 Page(s):961 - 972

AbstractPlus | References | Full Text: PDF(1929 KB) IEEE JNL

12. **Resource management in software-programmable router operating systems**
Yan, D.K.Y.; Xiangjing Chen;
Selected Areas in Communications, IEEE Journal on
Volume 19, Issue 3, March 2001 Page(s):488 - 500

AbstractPlus | References | Full Text: PDF(164 KB) IEEE JNL

13. **Unbounded transactional memory**
Ananian, C.S.; Asanovic, K.; Kuszmaul, B.C.; Leiserson, C.E.; Lie, S.;
High-Performance Computer Architecture, 2005. HPCA-11. 11th International Symposium on
12-16 Feb. 2005 Page(s):316 - 327

AbstractPlus | Full Text: PDF(184 KB) IEEE CNF

14. **Optimizing Software Cache-coherent Cluster Architectures**
Xiaohan Qin; Baer, J.;
Supercomputing, 1998. SC98. IEEE/ACM Conference on
07-13 Nov. 1998 Page(s):25 - 25

AbstractPlus | Full Text: PDF(360 KB) IEEE CNF

15. **Measuring VAX 8800 performance with a histogram hardware monitor**
Clark, D.W.; Bannon, P.J.; Keller, J.B.;
Computer Architecture, 1988. Conference Proceedings. 15th Annual International Symposium on
30 May-2 June 1988 Page(s):176 - 185

AbstractPlus | Full Text: PDF(712 KB) IEEE CNF

16. **The S3.mp scalable shared memory multiprocessor**
Nowatzyk, A.; Aybay, G.; Browne, M.; Kelly, E.; Lee, D.; Parkin, M.;
System Sciences, 1994. Vol. I: Architecture, Proceedings of the Twenty-Seventh Hawaii Internation Conference on
Volume 1, 4-7 Jan. 1994 Page(s):144 - 153

AbstractPlus | Full Text: PDF(928 KB) IEEE CNF

17. **Performance characterization of a quad Pentium Pro SMP using OLTP workloads**
Keeton, K.; Patterson, D.A.; Yong Qian He; Raphael, R.C.; Baker, W.E.;

Computer Architecture, 1998. Proceedings. The 25th Annual International Symposium on
27 June-1 July 1998 Page(s):15 - 26

AbstractPlus | Full Text: PDF(100 KB) IEEE CNF

18. **Timing analysis of block replacement algorithms on disk caches**
Rajamoni, R.; Bhagavathula, R.; Pendse, R.;
Circuits and Systems, 2000. Proceedings of the 43rd IEEE Midwest Symposium on
Volume 1, 8-11 Aug. 2000 Page(s):408 - 411 vol.1

AbstractPlus | Full Text: PDF(320 KB) IEEE CNF

19. **Asynchronous resource management**
Vajracharya, S.; Chavarria-Miranda, D.G.;
Parallel and Distributed Processing Symposium., Proceedings 15th International
23-27 April 2001 Page(s):9 pp.

AbstractPlus | Full Text: PDF(216 KB) IEEE CNF

20. **Scheduler-based DRAM energy management**
Delaluz, V.; Sivasubramaniam, A.; Kandemir, M.; Vijaykrishnan, N.; Irwin, M.J.;
Design Automation Conference, 2002. Proceedings. 39th
10-14 June 2002 Page(s):697 - 702

AbstractPlus | Full Text: PDF(833 KB) IEEE CNF

21. **Creating a national lab shared storage infrastructure**
Karpoff, W.;
Parallel and Distributed Processing Symposium., Proceedings International, IPDPS 2002, Abstracts and CD-ROM
15-19 April 2002 Page(s):55 - 65

AbstractPlus | Full Text: PDF(433 KB) IEEE CNF

22. **Design considerations for a general-purpose microprocessor**
Maytal, B.; Iacobovici, S.; Alpert, D.B.; Biran, D.; Levy, J.; Tov, S.Y.;
Computer
Volume 22, Issue 1, Jan. 1989 Page(s):66 - 76

AbstractPlus | Full Text: PDF(1000 KB) IEEE JNL

23. **The MIT Alewife Machine**
Agarwal, A.; Bianchini, R.; Chaiken, D.; Chong, F.T.; Johnson, K.L.; Kranz, D.; Kubiatowicz, J.D.; Beng-Hong Lim; Mackenzie, K.; Yeung, D.;
Proceedings of the IEEE
Volume 87, Issue 3, March 1999 Page(s):430 - 444

AbstractPlus | References | Full Text: PDF(392 KB) IEEE JNL

24. **Prefetching into smart-disk caches for high performance media servers**
Triantafillou, P.; Harizopoulos, S.;
Multimedia Computing and Systems, 1999. IEEE International Conference on
Volume 1, 7-11 June 1999 Page(s):500 - 505 vol.1

AbstractPlus | Full Text: PDF(612 KB) IEEE CNF

25. **Design and implementation of a caching system for streaming media over the Internet**
Bommaiah, E.; Guo, K.; Hofmann, M.; Paul, S.;
Real-Time Technology and Applications Symposium, 2000. RTAS 2000. Proceedings. Sixth IEEE
31 May-2 June 2000 Page(s):111 - 121

AbstractPlus | Full Text: PDF(356 KB) IEEE CNF

View: **1-25** | 26-50 | 51-75 | 76-96

Multiprocessor cache analysis using ATUM

Sites, R.L. Agarwal, A.
Digital Equipment Corp., Hudson, MA, USA;

This paper appears in: **Computer Architecture, 1988. Conference Proceedings. 15th Annual International Symposium on**
Publication Date: 30 May-2 June 1988
On page(s): 186 - 195
Meeting Date: 05/30/1988 - 06/02/1988
Location: Honolulu, HI
INSPEC Accession Number:3228434
DOI: 10.1109/ISCA.1988.5228
Posted online: 2002-08-06 15:52:23.0

Abstract
A tracing facility called ATUM-2 that allows the capture of large address traces of multiprocessors is described. The method is based on a previous scheme called address tracing using microcode (ATUM) for single processors (see ibid., vol.13, p.119-27, (1986)). In ATUM, the microcode of a machine is modified to record the address of the **memory** references as a side effect of normal execution. The addresses are recorded in a reserved portion of main **memory**, and periodically transferred to disk. The ATUM-2 implementation on a VAX 8350 multiprocessor is described and the use of the resulting traces to analyze physical versus virtual addressing of large **caches**, process-identifier hashing in virtual **caches**, **cache** interference between multiple processes, **cache** interference between multiple CPUs, process affinity, and semaphore usage in writeback **caches** is reported on

Index Terms
Inspec
Controlled Indexing
computer architecture multiprocessing systems storage allocation storage management

Non-controlled Indexing
ATUM-2 VAX 8350 multiprocessor address tracing using microcode **cache** interference **memory** references multiprocessor **cache** analysis process affinity process-identifier hashing tracing facility
Author Keywords
Not Available

References

No references available on IEEE Xplore.

Citing Documents

1 Two fast and high-associativity cache schemes, Chenxi Zhang; Xiaodong Zhang; Yong Yan
Micro, IEEE
On page(s): 40-49, Volume: 17, Issue: 5, Sep/Oct 1997
Abstract | Full Text: PDF (124)

2 Trace Factory: generating workloads for trace-driven simulation of shared-bus multiprocessors, Giorgi, R.; Prete, C.A.; Prina, G.; Ricciardi, L.
Concurrency, IEEE [see also IEEE Parallel & Distributed Technology]
On page(s): 54-68, Volume: 5, Issue: 4, Oct-Dec 1997
Abstract | Full Text: PDF (236)

3 Improving performance of large physically indexed caches by decoupling memory addresses from cache addresses, Rui Min; Yiming Hu
Computers, IEEE Transactions on
On page(s): 1191-1201, Volume: 50, Issue: 11, Nov 2001
Abstract | Full Text: PDF (3100)

View Search Results | Next Article

Cost-efficient memory architecture design of NAND flash memory embedded systems

Park, C. Seo, J. Seo, D. Kim, S. Kim, B.
SAMSUNG Electronics,Co., Ltd.

This paper appears in: **Computer Design, 2003. Proceedings. 21st International Conference on**
Publication Date: 13-15 Oct. 2003
On page(s): 474 - 480
Number of Pages: xxii+563
ISSN: 1063-6404
INSPEC Accession Number:7946671
DOI: 10.1109/ICCD.2003.1240943
Posted online: 2003-10-27 09:54:46.0

Abstract

NAND flash **memory** has become an Indispensable component in embedded systems because of its versatile features such as nonvolatility, solid-state reliability, low cost and high density. Even though NAND flash **memory** gains popularity as data storage, it also can be exploited as code **memory** for XIP (execute-in-place). We present a cost-efficient **memory** architecture, which incorporates NAND flash **memory** into an existing **memory** hierarchy for code execution. The usefulness of the proposed approach is demonstrated with real embedded workloads on a real hardware prototyping board.

Index Terms

Inspec

Controlled Indexing

NAND circuits cache storage embedded systems flash memories logic design memory architecture memory expansion boards

Non-controlled Indexing

NAND flash memory XIP code memory cost-efficient memory architecture design embedded systems execute-in-place memory hierarchy real hardware prototyping board

Author Keywords

Not Available

References

No references available on IEEE Xplore.

Citing Documents

No citing documents available on IEEE Xplore.

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L8: Entry 1 of 77 File: PGPB Jul 7, 2005

PGPUB-DOCUMENT-NUMBER: 20050149688
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20050149688 A1

TITLE: Computer system and a method of assigning a storage device to a computer

PUBLICATION-DATE: July 7, 2005

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Kitamura, Manabu	Yokohama	CA	JP	
Yamagami, Kenji	Los Gatos		US	
Murakami, Tatsuya	Odawara		JP	

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	COUNTRY	TYPE CODE
Hitachi, Ltd.				03

APPL-NO: 11/ 072723 [PALM]
DATE FILED: March 7, 2005

RELATED-US-APPL-DATA:
Application 11/072723 is a continuation-of US application 10/095582, filed March 13, 2002, PENDING
Application 10/095582 is a continuation-of US application 09/642817, filed August 22, 2000, US Patent No. 6854034

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	DOC-ID	APPL-DATE
JP	11-241024	1999JP-11-241024	August 27, 1999

INT-CL: [07] G06 F 12/00

US-CL-PUBLISHED: 711/170; 711/112, 711/114, 711/113
US-CL-CURRENT: 711/170; 711/112, 711/113, 711/114

REPRESENTATIVE-FIGURES: 4

ABSTRACT:

A computer system which has a plurality of computers and a storage device subsystem connected to the plurality of computers. The storage device subsystem has a plurality of storage devices and a plurality of interfaces, through which the subsystem is connected to the computers. One of the plurality of computers has a management means for holding therein data indicative of the storage devices and a connection relationship between the computers and storage device subsystem. Each computer, when wanting a new device, informs the management means of its capacity and type. The management means receives its notification and selects one of the storage devices which satisfies the request. And the management means instructs the storage device subsystem to set predetermined data in such a manner that the computer can access the

selected device. The management means also returns predetermined data to the computer as a device assignment requester, the assignment requester computer modifies setting thereof to allow the computer in question can use the assigned device.

Previous Doc Next Doc Go to Doc#

L8: Entry 5 of 77 File: PGPB Jul 7, 2005

PGPUB-DOCUMENT-NUMBER: 20050149671
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20050149671 A1

TITLE: Disk array apparatus and method for controlling the same

PUBLICATION-DATE: July 7, 2005

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Suzuki, Katsuyoshi	Odawara		JP	
Hirasawa, Akihisa	Odawara		JP	

APPL-NO: 11/ 056002 [PALM]
DATE FILED: February 14, 2005

RELATED-US-APPL-DATA:
Application 11/056002 is a continuation-of US application 10/659398, filed September 11, 2003, PENDING

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	DOC-ID	APPL-DATE
JP	2003-145111	2003JP-2003-145111	May 22, 2003

INT-CL: [07] G06 F 12/00

US-CL-PUBLISHED: 711/114
US-CL-CURRENT: 711/114

REPRESENTATIVE-FIGURES: 12

ABSTRACT:

An apparatus includes a controller and a plurality of disk drives. The controller has a communication control unit for accepting a data input/output request, a disk controller unit for controlling a disk drive, and a cache memory for temporarily storing data transferred between the communication control unit and the disk controller unit. The plurality of disk drives has different communication interfaces and connected to the disk controller unit to communicate with the disk controller unit.

CROSS-REFERENCE TO RELATED APPLICATION

[0001] The present application is a continuation of application Ser. No. 10/659,398, filed Sep. 11, 2003 and is related to Japanese Patent Application No. 2003-145111, filed on May 22, 2003, the contents of which are incorporated herein by reference in its entirety.

L8: Entry 41 of 77 File: USPT Jun 21, 2005

US-PAT-NO: 6910102
DOCUMENT-IDENTIFIER: US 6910102 B2

TITLE: Disk storage system including a switch

DATE-ISSUED: June 21, 2005

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Matsunami; Naoto	Sagamihara			JP
Oeda; Takashi	Sagamihara			JP
Yamamoto; Akira	Sagamihara			JP
Mimatsu; Yasuyuki	Fujisawa			JP
Sato; Masahiko	Odawara			JP

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Hitachi, Ltd.	Tokyo			JP	03

APPL-NO: 10/ 769922 [PALM]
DATE FILED: February 3, 2004

PARENT-CASE:
This is a continuation application of U.S. Ser. No. 10/405,645, filed on Apr. 3, 2003 now U.S. Pat. No. 6,851,029, which is a continuation application of U.S. Ser. No. 10/095,581, filed Mar. 13, 2002, now U.S. Pat. No. 6,701,411, which is a continuation application of U.S. Ser. No. 09/468,327, filed on Dec. 21, 1999, now U.S. Pat. No. 6,542,961. This application is related to U.S. Ser. No. 10/095,578, filed Mar. 13, 2002.

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
JP	10-364079	December 22, 1998

INT-CL: [07] G06F01200

US-CL-ISSUED: 711/114; 711/112, 711/130, 711/161, 711/162, 711/170, 714/6, 710/10, 709/220, 709/221, 709/222
US-CL-CURRENT: 711/114; 709/220, 709/221, 709/222, 710/10, 711/112, 711/130, 711/161, 711/162, 711/170, 714/6

FIELD-OF-SEARCH: 711/114, 711/112, 711/130, 711/161, 711/162, 711/170, 714/6, 710/10, 709/220, 709/223, 709/222

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5140592	August 1992	Idelman et al.	714/5
☐	5237658	August 1993	Walker et al.	710/38
☐	5257391	October 1993	DuLac et al.	710/10
☐	5423046	June 1995	Nunnelley et al.	711/114
☐	5457703	October 1995	Kakuta et al.	714/766
☐	5517662	May 1996	Coleman et al.	709/201
☐	5574950	November 1996	Hathorn et al.	710/8
☐	5581735	December 1996	Kajitani et al.	711/169
☐	5606359	February 1997	Youden et al.	725/88
☐	5619690	April 1997	Matsumani et al.	707/200
☐	5729763	March 1998	Leshem	710/38
☐	5752256	May 1998	Fujii et al.	710/220
☐	5835694	November 1998	Hodges	714/6
☐	5974503	October 1999	Venkatesh et al.	711/114
☐	6078990	June 2000	Frazier	711/114
☐	6098119	August 2000	Surugucchi et al.	710/10
☐	6098129	August 2000	Fukuzawa et al.	710/65
☐	6098199	August 2000	Barkin	2/159
☐	6105122	August 2000	Muller et al.	712/1
☐	6138176	October 2000	McDonald et al.	710/241
☐	6148349	November 2000	Chow et al.	710/33
☐	6173374	January 2001	Heil et al.	711/148
☐	6247077	June 2001	Muller et al.	710/74
☐	6253283	June 2001	Yamamoto	711/114
☐	6256740	July 2001	Muller et al.	713/201
☐	6263374	July 2001	Olnowich et al.	709/253
☐	6289376	September 2001	Taylor et al.	709/209
☐	6493750	December 2002	Mathew et al.	709/220
☐	6542961	April 2003	Matsunami et al.	711/114

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
980 041	February 2000	EP	
06-309186	November 1994	JP	
08/328760	December 1996	JP	
09-198308	July 1997	JP	

OTHER PUBLICATIONS

Microsoft Computer Dictionary, Forth Edition, p. 312, definition of the term "node," 1999.

"A Case for Redundant Arrays of Inexpensive Disks (RAID)", Proc. ACM SIGMOD, Jun. 1988, D. Patterson et al, pp. 109-116.
Serial SCSI Finally Arrives on the Market, Nikkei Electronics, No. 639, 1995, p. 79.
Chiang et al, "Implementation of STARNET: A WDM Computer Communications Network," IEEE, pp. 824-839, Jun. 1996.

ART-UNIT: 2186

PRIMARY-EXAMINER: Elmore; Stephen

ATTY-AGENT-FIRM: Mattingly, Stanger, Malur & Brundidge, P.C.

ABSTRACT:

A disk storage system containing a storage device having a record medium for holding the data, a plurality of storage sub-systems having a controller for controlling the storage device, a first interface node coupled to a computer using the data stored in the storage sub-systems, a plurality of second interface nodes connected to the storage sub-systems, a switch connecting to a first interface node and a plurality of second interface nodes to perform frame transfer therebetween based on node address information added to the frame. The first interface node has a configuration table to store structural information for the memory storage system and in response to the frame sent from the computer, analyzes the applicable frame, converts information relating to the transfer destination of that frame based on structural information held in the configuration table, and transfers that frame to the switch.

32 Claims, 30 Drawing figures

Previous Doc Next Doc Go to Doc#

L8: Entry 63 of 77 File: USPT Nov 11, 2003

US-PAT-NO: 6647461
DOCUMENT-IDENTIFIER: US 6647461 B2

TITLE: Disk array controller, its disk array control unit, and increase method of the unit

DATE-ISSUED: November 11, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Fujimoto; Kazuhisa	Kokubunji			JP
Kanai; Hiroki	Higashiyamoto			JP
Fujibayashi; Akira	Kokubunji			JP
Sakurai; Wataru	Odawara			JP

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Hitachi, Ltd.	Tokyo			JP	03

APPL-NO: 10/ 335899 [PALM]
DATE FILED: January 3, 2003

PARENT-CASE:
The present application is a continuation of application Ser. No. 10/234,471, filed Sep. 5, 2002; now U.S. Pat. No. 6,519,680 which is a continuation of application Ser. No. 09/663,379, filed Sep. 15, 2000, now U.S. Pat. No. 6,477,619, the contents of which are incorporated herein by reference.

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
JP	2000-072469	March 10, 2000

INT-CL: [07] G06 F 12/02

US-CL-ISSUED: 711/114; 711/113, 711/148, 710/313, 710/316
US-CL-CURRENT: 711/114; 710/313, 710/316, 711/113, 711/148

FIELD-OF-SEARCH: 711/113, 711/114, 711/148, 710/313, 710/316

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5603005	February 1997	Bauman et al.	710/317
☐	5680640	October 1997	Ofek et al.	709/100

☐	5841775	November 1998	Huang	340/825.29
☐	5960455	September 1999	Bauman	711/120
☐	6006296	December 1999	Gold et al.	710/100
☐	6085333	July 2000	DeKoning et al.	714/7
☐	6092155	July 2000	Olnowich	709/200
☐	6256749	July 2001	Kakuta et al.	714/6
☐	6385681	May 2002	Fujimoto et al.	710/316
☐	6425049	July 2002	Yamamoto et al.	711/112
☐	6477619	November 2002	Fujimoto	
☐	2001/0001325	May 2001	Fujimoto et al.	711/114
☐	2002/0091898	July 2002	Matsunami et al.	711/114

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
1166693	March 1999	JP	

ART-UNIT: 2187

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ABSTRACT:

A disk array controller is made up of multiple disk array control units for implementing the data read/write operation and each having channel IF units, disk IF units, cache memory units and shared memory units. The disk array controller further includes inter connections for interconnecting the shared memory units and interconnecting the cache memory units across the border of disk array control units. Thereby alleviating the deterioration of performance due to the data transfer between the disk array control units, when the multiple disk array control units are to be operated as a single disk array controller.

8 Claims, 22 Drawing figures

Previous Doc Next Doc Go to Doc#